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Learn & Implement your Innovative Project ideas with

Scientech Wireless Digital Communication System

Scientech 2281

Wireless Communication is fundamentally the art of communicating information without wires. In principle, wireless communication encompasses any number of techniques including underwater acoustic communication, semaphores, smoke signals, radio communication, and satellite communication, among others.

Thus the spotlight of this solution will focus on digital wireless communication. Every major wireless system being developed and deployed is built around digital communication including cellular communication, wireless local area networking, personal area networking, and high-definition television. This class is unique because it approaches wireless communication from the perspective of digital signal processing (DSP). No background in digital communication is assumed, though it would be helpful.

Scientech Wireless Digital Communication System is an practical approach to wireless digital communication. This approach makes wireless more concrete, avoids simply drowning in mathematics and useful for graduate students as well. Students build a practical foundation for further study and good preparation for industry.

Benefits

- It teaches digital communication from a digital signal processing perspective.
- Incorporate encoding, modulation, wireless channel, impairments, synchronization, demodulation, decoding etc.
- Practical based approach for more learning.
- Real time analysis of signal parameters, like gain, frequency etc.
- Analysis in both wired & wireless platform.
- Standard built-in labs for quick start.
- Build your own project in a short time.
- Get enter into Software Defined Radio field.
- Learner will be prepared for Communication Industry.

Features

- **Portable design**
- **Block level study and implementation**
- **Supported Communication Links:**
  - **Wired, Wireless and Optical (optional)**
- **Built-in simulation & real time software**
- **More than 20 built-in labs**
- **Internal & External data mode**
- **Baseband signal analysis of I & Q channel**
- **Dual 125 MSPS 10-bit D/A converters for I Channel and Q Channel**
- **Control setting for individual blocks**
- **Built-in RF-up converter**
- **Built-in RF-down converter**
- **User programmable**
- **Provision for external reference signal for PLL**
- **SMA connectors**
- **Built-in analog signal acquisition**
- **Logic Analyzer for digital signal analysis**
- **Constellation view for I & Q**
- **Study of impairments**
- **Digital Filters: Interpolation, Decimation and Raised Root Cosine with variable roll-off (α)**
- **Various Spreading codes**
- **Built-in low-noise frequency synthesizer**
- **Variable chip rate up to 10 Mchips/s**
- **JTAG USB connector for FPGA configuration**
- **USB2.0 interface**
- **2 Year Warranty**

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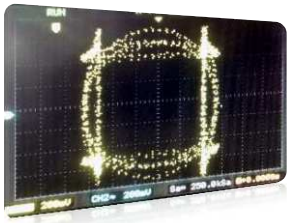
Real-Time Lab :

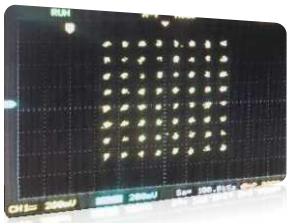
Scope of Learning

- To study Digital Communication Fundamentals using Simulation software
- To study RF frequency Spectrum analysis
- To study the Un-modulated carrier for Transmission by applying different signals like constant data / sine wave / cosine wave at I channel and Q channel.
- To study the concept of Pulse Shaping to improve Spectral Efficiency.
- Study about Digital FIR Filters.
  - RRC Filter.
  - Interpolation, Decimation [Low Pass Filters].
- To study & analyze baseband modulation techniques in time & frequency domain - BPSK, DBPSK, QPSK, DQPSK, OQPSK, π/4-QPSK,π/4 DQPSK, 8PSK, 8QAM, 16PSK, 16QAM, 16APSK, 32QAM, 32APSK, 64QAM, 128QAM
- To study about Direct Sequence Spread Spectrum System(DSSS),PN codes, types of PN codes, Chip Rate, Spreading Factor, Processing Gain.
- To study about Single Carrier Transmitter, Multi Carrier Transmitter.
- To study and analyze OFDM modulation, Sub-carriers, Symbol Rate, Bandwidth Efficiency.
- To study and analyze Convolution Encoder, Interleaver and De-interleaver.
- To study Digital Communication using wired, wireless & optical link (optional)

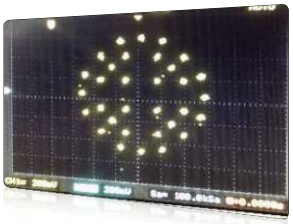


OQPSK Constellation

QPSK Constellation

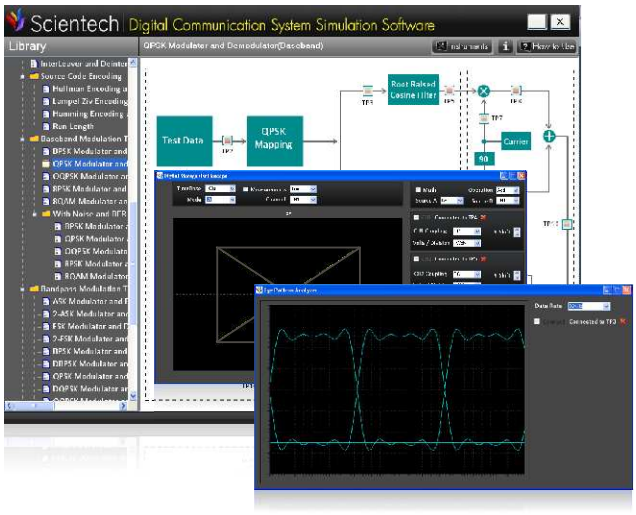


64-QAM Constellation



32-APSK Constellation

Digital Communication System Simulation Software



Simulation Lab :

Scope of Learning

- Basics (Signal Source,Pulse, Data Generator and Delay)
- Math Operation (Adder, Subtractor, Multiplier)
- Line Encoding and Decoding (Unipolar, polar, Bipolar, Manchester)
- PCM and DPCM Transmitter and Receiver
- A-Law and μ-law Companding
- 2-Channel TDM-PCM Multiplexer, Randomizer and Derandomizer, Convolution Encoding
- Modulator and Demodulator (Delta, Adaptive Delta, First Order Delta, Second Order Delta, PPM, PWM)
- Block Interleaver and Deinterleaver
- Source Code Encoding (Huffman, Lampel Ziv, Hamming, Run Length)
- Baseband and Bandpass Modulation Techniques with Noise and BER Measurement
- Signal Processing in Communication (Signals, Filter, Transformation, Processors, Applications)
- CDMA-DSSS, OFDM Transmitter and Receiver, BER Concept

RF Analog Fiber Optic Transmitter and Receiver Link (optional)

Optical

- Operating wavelenth	: 1310 nm ± 2 nm 1550 nm ± 2 nm
- Laser Diode	: Class 3A
- Output Power	: +3dBm ± 0.5dBm

RF Channel

- Modulation Bandwidth	: 100 MHz to 3.0 GHz
- Flatness (Max)	: ± 2.0dB

General

- Power Supply	: +8.0 to +24Vdc, 350mA max
- Optical Input Receptacle	: Pigtail, FC/APC, SC/APC
- RF Output Connector	: SMA (f), 50 ohm
- DC Connector	: DB-15

Setup with Fiber Optics Link

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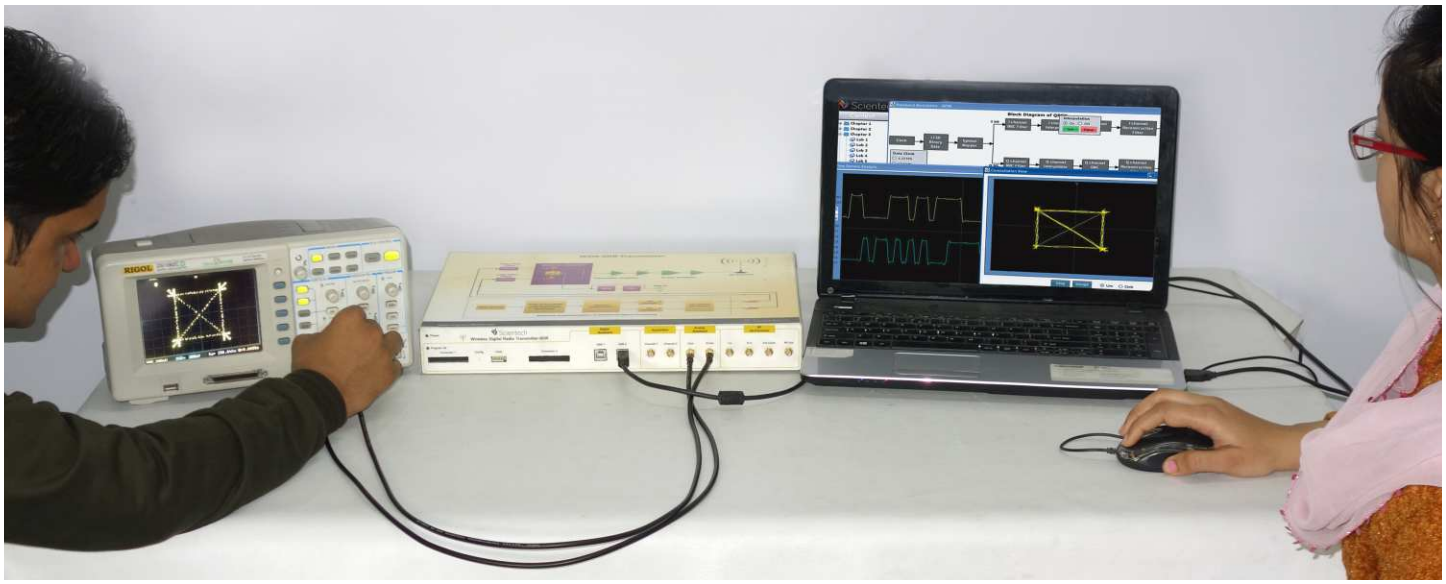
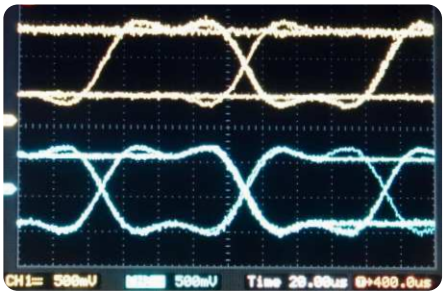


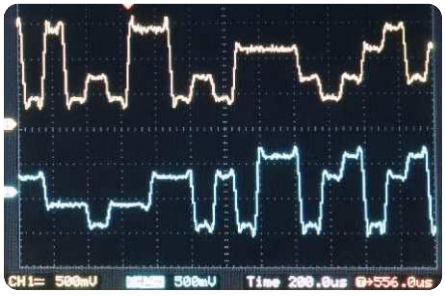
Wireless Digital Communication System-Transmitter

Technical Specifications

- Maximum Data Rate: 10 Mbps
- Device Xilinx FPGA Spartan3E XC3S500E
- Dual 125 MSPS 10-bit D/A converters for I Channel and Q Channel
- 6-pole Butterworth clock rejection filters
- Maximum bandwidth: +/- 13 MHz @±0.4dB ripple
- DAC clock rejection @ 40 MHz > 84 dBc
- Output voltage: 1Vpp with 0.85V DC bias
- JTAG USB connector for FPGA configuration
- Standard built-in Modulations like BPSK, DBPSK, QPSK, OQPSK, DQPSK, π/4 QPSK, π/4DQPSK, 8PSK, 8QAM, 16PSK, 16QAM, 16APSK, 32QAM, 32APSK, 64QAM, 128QAM
- Digital Filters: Interpolation, Decimation and Raised Root Cosine with variable roll-off (α)
- Built-in real time sSoftware with USB 2.0 interface
- Built-in Data Generator as test pattern
- External Digital Interface connector for expansion
- Programmable chip rates up to 10 Mchip/s
- Spreading codes:
  - Gold sequences (up to 2^{23} chips)
  - Maximal length sequences, (max length 2^{23} chips)
  - Barker codes (length 11, 13)
- 2.025 - 2.5GHz Quadrature Modulator
- Low-noise frequency synthesizer can be tuned over entire range by steps of 100, 31.25 or 25 KHz
- 8 preset frequencies for fast (<2ms) local oscillator frequency tuning
- Selectable internal / external 10 MHz frequency reference for the frequency synthesizer
- Fixed 10 MHz Oscillator(±2.5PPM)
- Gold platted SMA(F) connectors for Base-band and RF
- Built-in channel impairments generation: AWGN and Frequency Offset (Doppler)
- Data Acquisition Section: (for both Transmitter & Receiver)
  - Analog Channel: 2 (CH1 & CH2)
  - Resolution: 8-bit
  - Digital Channel: 8 (D0 – D7)
  - Maximum Real-time Sampling: 100MSPS (Analog + Digital Channel Simultaneously)
  - Memory Depth: 2K
  - Mode: Y-T (Time-domain View) & X-Y (Constellation View)



Eye diagram



Multilevel Signal

π/4 DQPSK Constellation

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Wireless Digital Communication System-Receiver

Technical Specifications

- Maximum output data rate: 10 Mbps
- Device Xilinx FPGA Spartan3E XC3S500E
- Dual 10-bit Analog-to-Digital converters, 40 Msamples/s
- Internal 40 MHz ADC sampling clock
  - Baseband filtering options: Wideband applications (< 26 MHz)
- JTAG USB Connector for FPGA configuration
- Built-in real time Software with USB 2.0 interface
- 2.025 – 2.5 GHz Receiver
- Sensitivity: -56 dBm RF input for full scale 10-bit output samples
- Built-in RF AGC, 70 dB dynamic range
- Low phase-noise frequency synthesizer can be tuned over entire range by steps of 100, 31.25, or 25 KHz
- 8 preset frequencies for fast (<2ms) local oscillator frequency tuning
- Selectable internal / external 10 MHz frequency reference for the frequency synthesizer
- SMA connectors
- Direct Sequence Spread-Spectrum demodulator
- Variable chip rate up to 10 Mchips/s
- Spreading codes:
  - Gold sequences (up to 2^{23} chips)
  - Maximal length sequences, (max length 2^{23} chips)
  - Barker codes (length 11, 13)
- BPSK, QPSK selectable
- Demodulation performances: within 1.5 dB from theory at threshold SNR of 5 dB
- Sequential code search
- Receiver lock monitoring using software
- External Digital Interface connector for expansion
- Measures actual bit errors while a known PRBS-11 pseudo-random test sequence is being transmitted

Included Accessories

Transmitter Power Supply	:	1 no.
Receiver Power Supply	:	1 no.
USB to USB cable	:	2 nos.
SMA male to SMA male cable	:	3 nos.
SMA to BNC cable	:	3 nos.
Xilinx USB JTAG cable (with CD)	:	1 nos.
Serial to USB converter dongle	:	1 no.
Antenna	:	2 nos.
FRC Cable 40 pin	:	1 no.
Transmitter external card	:	1 no.
Receiver external card	:	1 no.
Serial Cable	:	1 no.
Mains cord Detachable	:	2 nos.
Fixed 10 MHz Oscillator(±2.5PPM) with Power Adaptor	:	2 nos.
Xilinx ISE Webpack Software CD	:	1 no.
Learning Material (CD)	:	1 no.

Optional

RF Analog Optical Transmitter and Receiver Link

3.3 GHz Handheld Spectrum Analyzer MSA458

*Computer is not included along with TechBook Scientech 2281

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